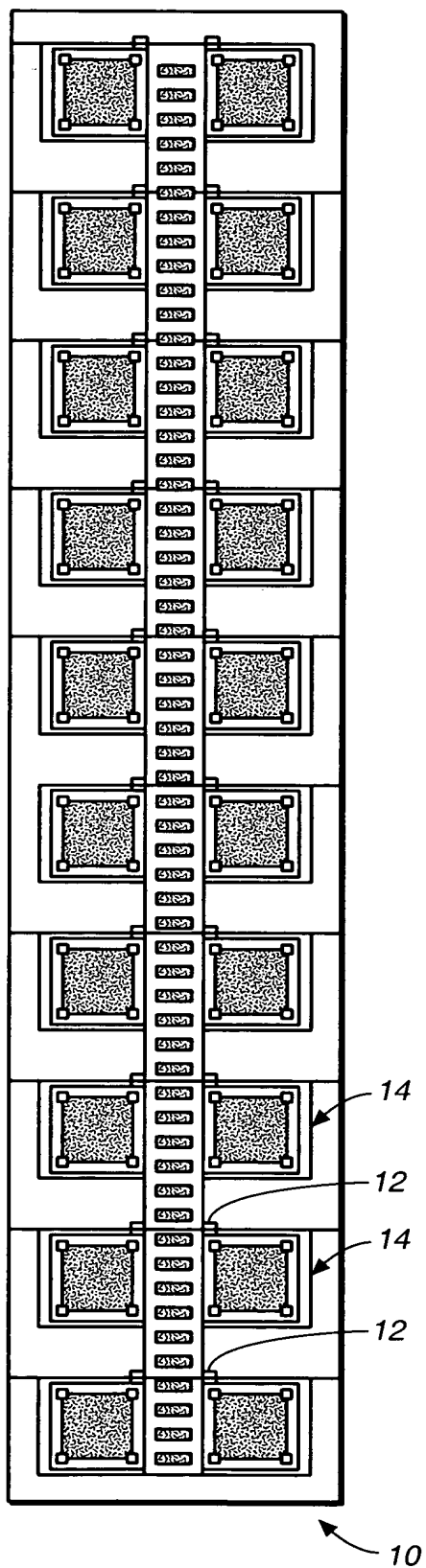


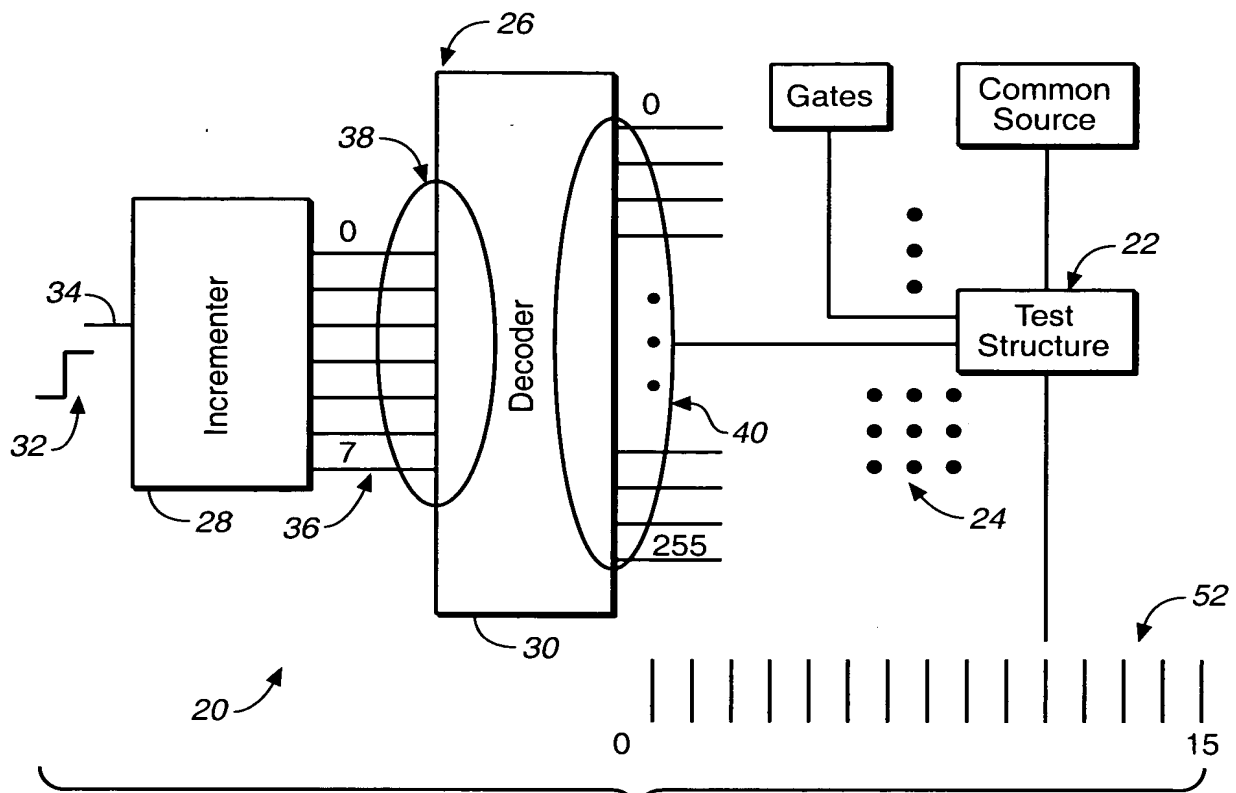
03-1169

1 / 3

FIG._1



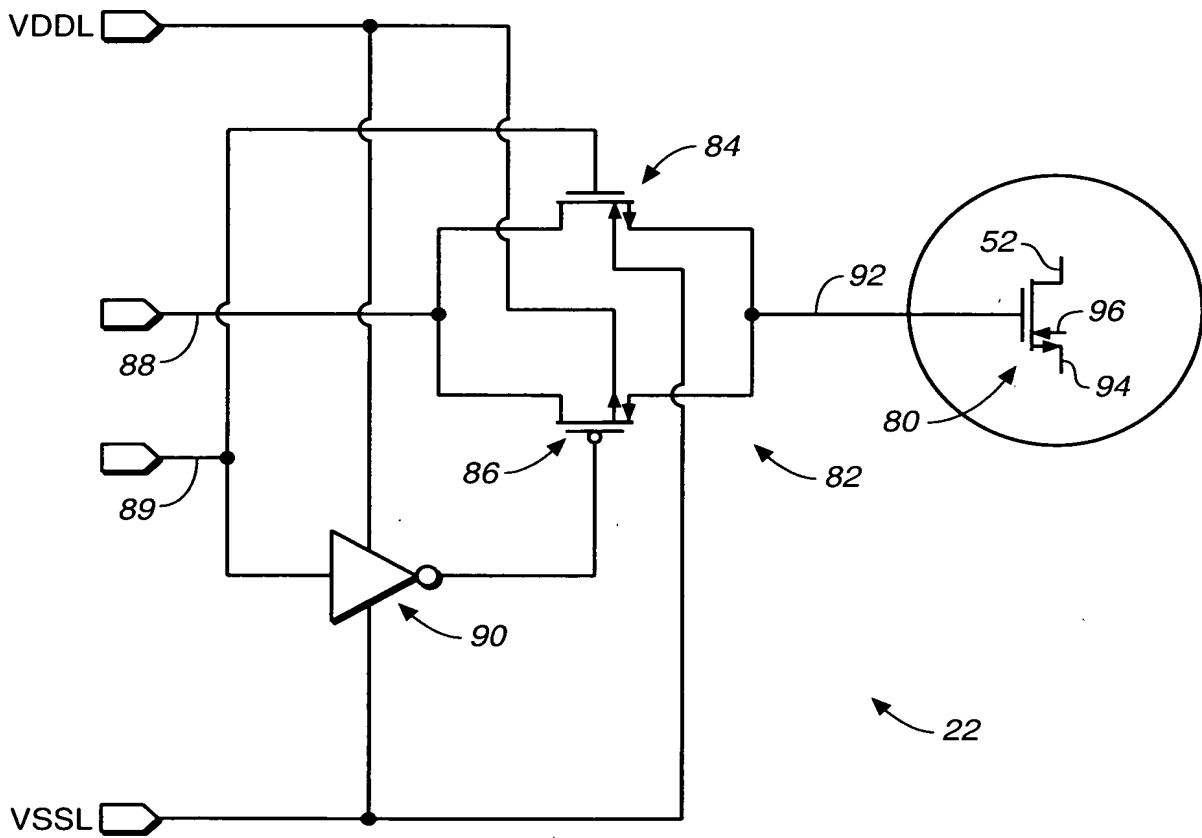
2 / 3

**FIG._2**

Outputs Trigger	7	6	5	4	3	2	1	0
1 st	0	0	0	0	0	0	0	1
2 nd	0	0	0	0	0	0	1	0
3 rd	0	0	0	0	0	0	1	1
256 th	1	1	1	1	1	1	1	1

FIG._3

Input Seq. →		1st	2nd	3rd			256th
Inputs: Address Lines	0	0	1	0	...		1
	1	0	0	1			1
	2	0	0	0			1
	3	0	0	0			1
	4	0	0	0			1
	5	0	0	0			1
	6	0	0	0			1
	7	0	0	0			1

FIG._4**FIG._5**